Claims

What is claimed is:

1. A computer system, comprising:

   a delay array arranged to generate an output signal that is delayed with respect to an input signal by an amount indicated by a delay code provided to the delay array;

   a shift controller operatively connected to the delay array and arranged to update the delay code dependent on a phase comparison of the input signal and the output signal; and

   a detection circuit arranged to monitor the delay code,

   wherein, the detection circuit, in response to a predetermined condition of the delay code, causes a self-reset of the delay code to a value different than that of a value of the delay code at one of a previous reset and an initial startup of the delay array.

2. The computer system of claim 1, wherein the shift controller comprises the detection circuit.

3. The computer system of claim 1, wherein the shift controller comprises a phase comparator, and wherein the phase comparator is a D flip-flop.

4. The computer system of claim 1, further comprising:

   a shift register arranged to store the delay code and operatively connected to the shift controller.

5. The computer system of claim 1, wherein a value of the self-reset delay code indicates more delay being needed than a value of the delay code at one of the reset and the startup of the delay array.

6. The computer system of claim 1, wherein a value of the self-reset delay code indicates less delay being needed than a value of the delay code at one of the reset and the startup of the delay array.

7. The computer system of claim 1, further comprising:

a strobe delay line arranged to delay a strobe signal by an amount of delay indicated by the delay code.

8. The computer system of claim 7, further comprising:

a memory arranged to output the strobe signal to the strobe delay line.

9. The computer system of claim 8, further comprising:

a buffer having a clock input operatively connected to the delayed strobe signal,

wherein the memory is further arranged to selectively output data to the buffer.

10. The computer system of claim 1, wherein at least one of the delay array, the shift controller, and the detection circuit are digital.

11. A computer system, comprising:

means for delaying an input signal to generate an output signal, the means for delaying being dependent on a delay code indicative of an amount of delay by which to delay the input signal;

means for comparing phases of the input signal and the output signal;

means for updating the delay code dependent on the means for comparing phases;

means for monitoring the delay code; and

means for resetting the delay code in response to a detected predetermined condition of the delay code, wherein the delay code is reset to a

value different than a value of the delay code present at one of a previous reset and an initial startup of the means for delaying.

12. The computer system of claim 11, further comprising:

means for storing the delay code.

13. The computer system of claim 11, wherein the means for resetting is configured to reset the delay code to a value indicative of more delay being needed than as indicated by a value of the delay code present at one of the previous reset and the initial startup.

14. The computer system of claim 11, wherein the means for resetting is configured to reset the delay code to a value indicative of less delay being needed than as indicated by a value of the delay code present at one of the previous reset and the initial startup.

15. The computer system of claim 11, further comprising:

means for delaying an incoming signal from an external memory dependent on the delay code.

16. A method for performing delay locked loop operations, comprising:

delaying an input signal to generate an output signal, wherein the output signal is delayed with respect to the input signal by an amount indicated by a delay code;

comparing phases of the input signal and the output signal;

updating the delay code dependent on the comparing; and

monitoring the delay code for a predetermined condition,

wherein, in response to detecting the predetermined condition, resetting the delay code to a value different than a value of the delay code present at least at one of a previous reset and an initial startup of the delaying.

17. The method of claim 16, wherein the resetting comprises resetting the delay code to a value indicative of more delay being needed than as indicated by a value of the delay code present at least at one of the previous and the initial startup.

18. The method of claim 16, wherein the resetting comprises resetting the delay code to a value indicative of less delay being needed than as indicated by a value of the delay code present at least at one of the previous reset and the initial startup.

19. The method of claim 16, further comprising:

storing the delay code.

20. The method of claim 16, further comprising:

delaying an input strobe signal dependent on the delay code.